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NORMAN P SOLOWAY
HAYES SOLOWAY HENNESSEY GROSSMAN & HAGE
175 CANAL STREET
MANCHESTER, NH 03101

EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/222,524	Applicant(s) MATSUDA, SHUICHI
	Examiner Nitin Parekh	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 1998* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 21, 24, 27, 30, 33, 36, 39, 42, 45, 48, 51 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Rostoker (US Pat. 5399898), Yoshizaki (US Pat. 5475236) and Liang (US Pat. 5952726).

Regarding claim 21, APA discloses a semiconductor device comprising:

- a wiring substrate/tap automated bonding (TAB) substrate/film carrier (2 in Fig. 8) having a predetermined pattern of wiring formed on one surface and having a number of through-holes
- a semiconductor chip (1 in Fig. 8) disposed on the other surface of the wiring substrate having chip electrodes and a wiring layer (4 and 3 respectively in Fig. 8)
- a number of bumps disposed/formed respectively in through-holes (5/6 in Fig. 8) of the wiring substrate/disposed in conforming relationship with the chip electrodes and electrically connecting the wiring of the wiring substrate with the electrode, and
- a single external bump pad (2c in Fig. 8) for the bump electrically connected through the wiring layer to the chip electrodes

(Fig. 7 and 8; Specification pages 1-3).

APA fails to specify:

a) the semiconductor chip having at least one electrode set comprising two chip electrodes in a common wiring layer of the chip, and

b) arranging them from the edge of the chip towards its inner side.

a) Rostoker teaches using a semiconductor chip comprising a variety of internal connections and having an electrode set comprising two electrodes (222 c and d in chip 224; Fig. 2b) being connected to a common wiring layer (Fig. 2b; Col. 11, line 23-Col. 12, line 13) in a flip-chip assembly. Rostoker further teaches increasing the bond pad/bump density using predetermined bond size/spacing to 600 or 1000 I/O counts or more to achieve the desired external connection capability and increased bump connections for a given chip area (Fig. 6-7B; Col. 17, line 20- Col. 19, line 35).

Yoshizaki teaches using a semiconductor chip comprising an electrode set comprising two electrodes (201c in Fig. 7) being connected to a common wiring layer/pattern (204 in Fig. 7) in a flip-chip assembly. Yoshizaki further teaches connecting two electrodes to a single external bump/pad (22 in Fig. 7).

b) Liang teaches using a grid/pattern of chip electrodes/bump pads comprising ground, power-source and signal terminals in a in a flip-chip assembly having a variety of configurations with different parameters such as pitch/dimension, number of electrodes, etc. where the chip electrodes/pads are arranged from the edge of the chip towards it's inner side or parallel to the edge of the chip (Fig. 2: Col. 1, line 42; Col. 2, line 42; Fig. 4-6; Col. 5, line 1-45; Col. 2-5).

It would have been obvious to a person of ordinary skill in the art to incorporate a chip having an electrode set or two electrode sets comprising two electrodes in a common wiring layer of the semiconductor chip as taught by Rostoker and Yoshizaki and arranging them from the edge of the chip towards it's inner side as taught by Liang so that the internal connection density and bump stress distribution can be improved in APA.

Regarding claim 24, APA teaches substantially the entire claimed structure as applied to claim 21 above, except the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip.

Liang teaches using the chip electrodes comprising ground, power-source and signal terminals of the semiconductor chip in a flip-chip assembly (Fig. 4A-C; Col. 2-9; Fig. 1-7).

It would have been obvious to a person of ordinary skill in the art to incorporate the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip as taught by Liang so that the desired grounding and power/signal routing can be achieved in Rostoker, Yoshizaki and APA's device.

Regarding claim 45, APA teaches substantially the entire claimed structure as applied to claim 21 above, except the chip comprising at least two electrode sets each at least comprising at least two chip electrodes in the common wiring layer.

Rostoker further teaches increasing the bond pad/electrode/bump density using predetermined bond size/spacing to 600 or 1000 I/O counts or more to achieve the

desired external connection capability and increased bump/electrode connections for a given chip area (Fig. 6-7B; Col. 17, line 20- Col. 19, line 35).

It would have been obvious to a person of ordinary skill in the art to incorporate the chip comprising at least two electrode sets each at least comprising at least two chip electrodes in the common wiring layer as taught by Rostoker so that the internal connection density can be improved and the desired grounding, power and signal routing can be achieved in Yoshizaki, Liang and APA's device.

Regarding claim 27, APA teaches substantially the entire claimed structure as applied to claim 21 above, including the number of bumps (5/6 in Fig. 8 of APA) being disposed on the wiring of the wiring substrate (APA specification page 2, lines 12-18).

Regarding claim 30, APA teaches substantially the entire claimed structure as applied to claims 21 and 27 above, except the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip.

Liang further teaches using the chip electrodes comprising ground, power-source and signal terminals of the semiconductor chip in a flip-chip assembly (Fig. 4A-C; Col. 2-9; Fig. 1-7).

It would have been obvious to a person of ordinary skill in the art to incorporate the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip as taught by Liang so that

the desired grounding and power/signal routing can be achieved in Yoshizaki, Rostoker and APA's device.

Regarding claim 48, APA teaches substantially the entire claimed structure as applied to claim 27 above, except the chip comprising at least two electrode sets each at least comprising at least two chip electrodes in the common wiring layer.

Rostoker further teaches increasing the bond pad/electrode/bump density using predetermined bond size/electrode spacing to 600 or 1000 I/O counts or more to achieve the desired external connection capability and increased bump/electrode connections for a given chip area (Fig. 6-7B; Col. 17, line 20- Col. 19, line 35).

It would have been obvious to a person of ordinary skill in the art to incorporate the chip comprising at least two electrode sets each at least comprising at least two chip electrodes in the common wiring layer as taught by Rostoker so that the internal connection density can be improved and the desired grounding, power and signal routing can be achieved in Yoshizaki, Liang and APA's device.

Regarding claims 33, 36, 51, 39, 42 and 54, APA teaches substantially the entire claimed structure as applied to claims 21, 24, 45, 27, 30 and 48 respectively above, including the wiring substrate comprising the tap automated bonding/TAB (APA: 2 in Fig. 7 and 8; Specification pages 1 and 2).

3. Claims 22, 25, 28, 31, 34, 37, 40, 43, 46, 49, 52 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA, Rostoker (US Pat. 5399898), Yoshizaki (US Pat. 5475236) and Liang (US Pat. 5952726) as applied to claim 21 above, and further in view of Fulcher (US Pat. 5686764).

Regarding claim 22, APA, Rostoker, Yoshizaki and Liang teach substantially the entire claimed structure as applied to claim 21 above, except the chip electrodes being parallel to an edge of the chip and the wiring being bent at least one position.

Fulcher teaches using I/O, power/signal wiring layout with patterns of different dimensions, shapes where the wiring is bent at various positions (Fig. 4A; Col. 7, line 10) in a flip chip substrate/tape to optimize the spacing of wiring/traces and to reduce the signal interference and cross-talk (Fig. 3-8, Col. 3-5).

It would have been obvious to a person of ordinary skill in the art to arrange the chip electrodes being parallel to the edge of the chip and the wiring is bent at least one position as taught by Fulcher so that the spacing of wiring/traces can be optimized and the signal interference/cross-talk can be reduced in Rostoker, Yoshizaki, Liang and APA's device.

Regarding claim 25, APA, Rostoker, Yoshizaki and Liang teach substantially the entire claimed structure as applied to claim 22 above, except the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip.

Liang teaches using the chip electrodes comprising ground, power-source and signal terminals of the semiconductor chip in a flip-chip assembly (Fig. 4A-C; Col. 2-9; Fig. 1-7).

It would have been obvious to a person of ordinary skill in the art to incorporate the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip as taught by Liang so that the desired grounding and power/signal routing can be achieved in Rostoker, Yoshizaki, Fulcher and APA's device.

Regarding claim 46, APA teaches substantially the entire claimed structure as applied to claim 22 above, except the chip comprising at least two electrode sets each at least comprising at least two chip electrodes in the common wiring layer.

Rostoker further teaches increasing the bond pad/bump density using predetermined bond size/spacing to 600 or 1000 I/O counts or more to achieve the desired external connection capability and increased bump connections for a given chip area (Fig. 6-7B; Col. 17, line 20- Col. 19, line 35).

It would have been obvious to a person of ordinary skill in the art to incorporate the chip comprising at least two electrode sets each at least comprising at least two chip electrodes in the common wiring layer as taught by Rostoker so that the internal connection density can be improved and the desired grounding, power and signal routing can be achieved in Liang, Yoshizaki, Fulcher and APA's device.

Regarding claim 28, APA, Rostoker, Yoshizaki and Liang teach substantially the entire claimed structure as applied to claim 22 above, including the number of bumps (5/6 in Fig. 8 of APA) being disposed on the wiring of the wiring substrate (APA specification page 2, lines 12-18).

Regarding claim 31, APA, Rostoker, Yoshizaki and Liang teach substantially the entire claimed structure as applied to claims 22 and 28 above, except the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip.

Liang further teaches using the chip electrodes comprising ground, power-source and signal terminals of the semiconductor chip in a flip-chip assembly (Fig. 4A-C; Col. 2-9; Fig. 1-7).

It would have been obvious to a person of ordinary skill in the art to incorporate the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip as taught by Liang so that the desired grounding and power/signal routing can be achieved in Yoshizaki, Rostoker Fulcher and APA's device.

Regarding claim 49, APA, Rostoker, Yoshizaki and Liang teach substantially the entire claimed structure as applied to claims 28 and 22 above, except the chip comprising at least two electrode sets each at least comprising at least two chip electrodes in the common wiring layer.

Rostoker further teaches increasing the bond pad/electrode//bump density using predetermined bond size/electrode spacing to 600 or 1000 I/O counts or more to achieve the desired external connection capability and increased bump/electrode connections for a given chip area (Fig. 6-7B; Col. 17, line 20- Col. 19, line 35).

It would have been obvious to a person of ordinary skill in the art to incorporate the chip comprising at least two electrode sets each at least comprising at least two chip electrodes in the common wiring layer as taught by Rostoker so that the internal

connection density can be improved and the desired grounding, power and signal routing can be achieved in Liang, Yoshizaki, Fulcher and APA's device.

Regarding claims 34, 37, 52, 40, 43 and 55, APA teaches substantially the entire claimed structure as applied to claims 22, 25, 46, 28, 31 and 49 respectively above, including the wiring substrate comprising the tap automated bonding/TAB (APA: 2 in Fig. 7 and 8; Specification pages 1 and 2).

4. Claims 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 53 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA, Rostoker (US Pat. 5399898), Yoshizaki (US Pat. 5475236) and Liang (US Pat. 5952726) as applied to claim 21 above, and further in view of Bertolet et al. (US Pat. 5844317).

Regarding claim 23, APA, Rostoker, Yoshizaki and Liang teach substantially the entire claimed structure as applied to claim 21 above, except the wiring having an end width larger than an interelectrode distance between the chip electrodes.

Bertolet et al. teach using a variety of shapes/dimensions and end widths of wiring pattern/pad (Fig. 3) to achieve the desired bonding area and to improve the bonding strength.

It would have been obvious to a person of ordinary skill in the art to incorporate the wiring having an end width larger than an interelectrode distance between the chip electrodes as taught by Bertolet et al. so that the bonding area and bonding strength can be increased and bump stress distribution can be improved in Rostoker, Yoshizaki, Liang and APA's device.

Regarding claim 26, APA, Rostoker, Yoshizaki and Liang teach substantially the entire claimed structure as applied to claim 23 above, except the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip.

Liang teaches using the chip electrodes comprising ground, power-source and signal terminals of the semiconductor chip in a flip-chip assembly (Fig. 4A-C; Col. 2-9; Fig. 1-7).

It would have been obvious to a person of ordinary skill in the art to incorporate the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip as taught by Liang so that the desired grounding and power/signal routing can be achieved in Rostoker, Yoshizaki, Bertolet et al. and APA's device.

Regarding claim 47, APA, Rostoker, Yoshizaki and Liang teach substantially the entire claimed structure as applied to claim 21 above, except the chip comprising at least two electrode sets each at least comprising at least two chip electrodes in the common wiring layer.

Rostoker further teaches increasing the bond pad/bump density using predetermined bond size/spacing to 600 or 1000 I/O counts or more to achieve the desired external connection capability and increased bump connections for a given chip area (Fig. 6-7B; Col. 17, line 20- Col. 19, line 35).

It would have been obvious to a person of ordinary skill in the art to incorporate the chip comprising at least two electrode sets each at least comprising at least two chip electrodes in the common wiring layer as taught by Rostoker so that the internal connection density can be improved and the desired grounding, power and signal routing can be achieved in Yoshizaki, Liang, Bertolet et al. and APA's device.

Regarding claim 29, APA, Rostoker, Yoshizaki and Liang teach substantially the entire claimed structure as applied to claim 23 above, including the number of bumps (5/6 in Fig. 8 of APA) being disposed on the wiring of the wiring substrate (APA specification page 2, lines 12-18).

Regarding claim 32, APA, Rostoker, Yoshizaki and Liang teach substantially the entire claimed structure as applied to claims 22 and 28 above, except the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip.

Liang further teaches using the chip electrodes comprising ground, power-source and signal terminals of the semiconductor chip in a flip-chip assembly (Fig. 4A-C; Col. 2-9; Fig. 1-7).

It would have been obvious to a person of ordinary skill in the art to incorporate the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip as taught by Liang so that the desired grounding and power/signal routing can be achieved in Yoshizaki, Rostoker, Bertolet et al. and APA's device.

Regarding claim 50, APA, Rostoker, Yoshizaki and Liang teach substantially the entire claimed structure as applied to claim 23 and 29 above, except the chip comprising at least two electrode sets each at least comprising at least two chip electrodes in the common wiring layer.

Rostoker further teaches increasing the bond pad/electrode/bump density using predetermined bond size/electrode spacing to 600 or 1000 I/O counts or more to achieve the desired external connection capability and increased bump/electrode connections for a given chip area (Fig. 6-7B; Col. 17, line 20- Col. 19, line 35).

It would have been obvious to a person of ordinary skill in the art to incorporate the chip comprising at least two electrode sets each at least comprising at least two chip electrodes in the common wiring layer as taught by Rostoker so that the internal connection density can be improved and the desired grounding, power and signal routing can be achieved in Yoshizaki, Liang and APA's device.

Regarding claims 35, 38, 53, 41, 44 and 56, APA, Rostoker, Yoshizaki and Liang teaches substantially the entire claimed structure as applied to claims 23, 26, 47, 29, 32 and 50 respectively above, including the wiring substrate comprising the tap automated bonding/TAB (APA: 2 in Fig. 7 and 8; Specification pages 1 and 2).

Response to Arguments

5. Applicant's arguments filed on 03-13-03 have been fully considered but they are not persuasive.

A. Applicant contends that Rostoker and Yoshizaki do nor teach the electrodes being formed in a common wiring layer.

However, as explained above, Fig. 2b in Rostoker shows the electrode set comprising two electrodes (222 c and d) being connected to a common internal conductor/wiring layer of the chip (235a/224 in Fig. 2b; Col. 11, line 23-Col. 12, line 13).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

05-10-03

Steven Loke